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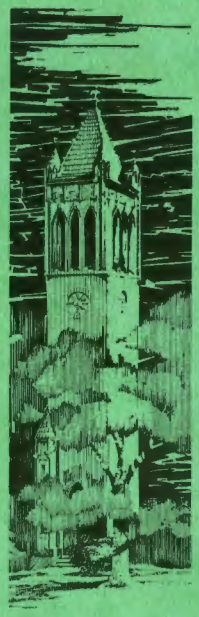

IOWA STATE UNIVERSITY

LOW NOISE NARROW-BAND AMPLIFICATION WITH FIELD EFFECT TRANSISTORS

by

Louis Mourlan, Jr. and Wayne A. Rhinehart

AMES LABORATORY

RESEARCH AND DEVELOPMENT REPORT

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LOW NOISE NARROW-BAND AMPLIFICATION WITH FIELD EFFECT TRANSISTORS

by

Louis Mourlan, Jr. and Wayne A. Rhinehart

February, 1965

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LOW NOISE NARROW-BAND AMPLIFICATION WITH FIELD EFFECT TRANSISTORS*

Louis Mourlam, Jr. and Wayne A. Rhinehart

ABSTRACT

Scientists and engineers are often confronted with the problem of detecting the presence of signal levels which approach the noise levels in available amplifying devices. This paper describes the factors which limit amplifier sensitivity and explains what the circuit designer can do to maximize sensitivity.

Low noise, narrow-band amplifier design, relative to the field effect transistor, is discussed and illustrated with a design example.

*This report is based on a MS thesis submitted by Louis Mourlam, Jr. February, 1965, to Iowa State University, Ames, Iowa.

INTRODUCTION

Scientists and engineers are often confronted with the problem of detecting the presence of signal levels which approach the noise levels in available amplifying devices. The ultimate limit of system performance in many experiments in nuclear research is the sensitivity of available amplifying instruments. A practical example is the problem of determining a complex impedance to an accuracy of one part per million by balancing an AC Kelvin bridge. This may well require that the null detector be able to sense an unbalance of 30-40 nano-volts. The accuracy of the balance condition is directly limited by the minimum detectable signal of the detector. Since such a bridge would be driven by a stable single frequency oscillator, the null detecting amplifier could be an extremely narrow-band instrument. The minimum detectable signal of such an instrument is limited by the random noise generated by the source impedance and within the amplifier itself.

Amplifiers capable of fulfilling the above requirements are in existence (1); however, there is always a need for improvement. Instruments using vacuum tubes are troubled with microphonic noise. Microphonic noise is a signal generated in the amplifier, usually the input tube, due to a physical vibration of the instrument. Such a reaction can result from simply slamming a laboratory door. The use of the nuvistor tube, specially constructed for low microphonics, has minimized this problem, but it still exists. The nuvistor amplifier requires feedback regulated filament and plate supplies to insure gain stability. These are the primary areas where improvement can be achieved.

The purpose of this investigation is to analyze the factors involved in the design of an improved amplifier using field effect transistors in the input stage. A specific design example is presented as an illustration of the generalized conclusions. The investigation is concluded with typical applications of the resultant low noise narrow-band amplifier.

THEORETICAL CONSIDERATIONS

Noise

Since noise is the primary adversary in the design of a sensitive amplifier, a clear understanding of the nature and source of noise is a necessity.

In the most general sense, noise in an amplifier can be defined as any signal other than the desired signal. The two major sources of unwanted signals in a sensitive amplifier are: 60 cps pickup at the input and random fluctuations generated at the input by the amplifier. The latter source is the most difficult to define and is usually the factor which limits amplifier sensitivity.

In all laboratories there is an abundance of 60 cps "transmitters", such as fluorescent lights and laboratory equipment which operates from the 60 cps mains. Unfortunately, a high input impedance amplifier is an excellent "receiver" of the externally generated 60 cps.

The sources of random fluctuations present at the amplifier input are not as easily defined as the 60 cps sources. Definition of such sources depends somewhat on the components used in the input circuit. For example, the noise mechanisms in vacuum tubes are different, in some respects, from those in transistors. Regardless of the circuit components used, thermal noise, often called Johnson noise, is always present. Johnson noise is due to the random motion of electrons through an electrical resistance. This random motion is caused by the thermal excitation of the electrons. Even if it was possible to build a noiseless amplifier, system resolution would be

limited by the thermal noise generated in the source resistance.

The root-mean-square value of thermal noise in a resistance R at room temperature can be calculated by the well-known equation:

$$E_n = 1.28 \cdot 10^{-10} \left[RB\right]^{\frac{1}{2}} \tag{1}$$

where B = noise bandwidth

It is important to note that the noise bandwidth, not the 3 db bandwidth, is specified.

The effective noise bandwidth of an amplifier is defined as the width of a rectangle whose length equals the mid-band power gain G_{mb} and whose area equals the area under the power gain G versus frequency curve (see Figure 1). The area equality can be stated mathematically as

$$BG_{mb} = \int_0^\infty G(f)\, df$$

or

$$B = \frac{1}{G_{mb}} \int_0^\infty G(f)\, df \tag{2}$$

Expressing power gain in terms of network voltages and impedances

$$G(f) = \frac{P_o}{P_i} = \frac{E_o^2(f)/R_o}{E_i^2(f)/R_i} \quad \text{and} \quad G_{mb} = \frac{E_o^2(f_{mb})/R_o}{E_i^2(f_{mb})/R_i}$$

where subscripts o refer to output, i to input and mb to midband.

Equation 2 then can be written:

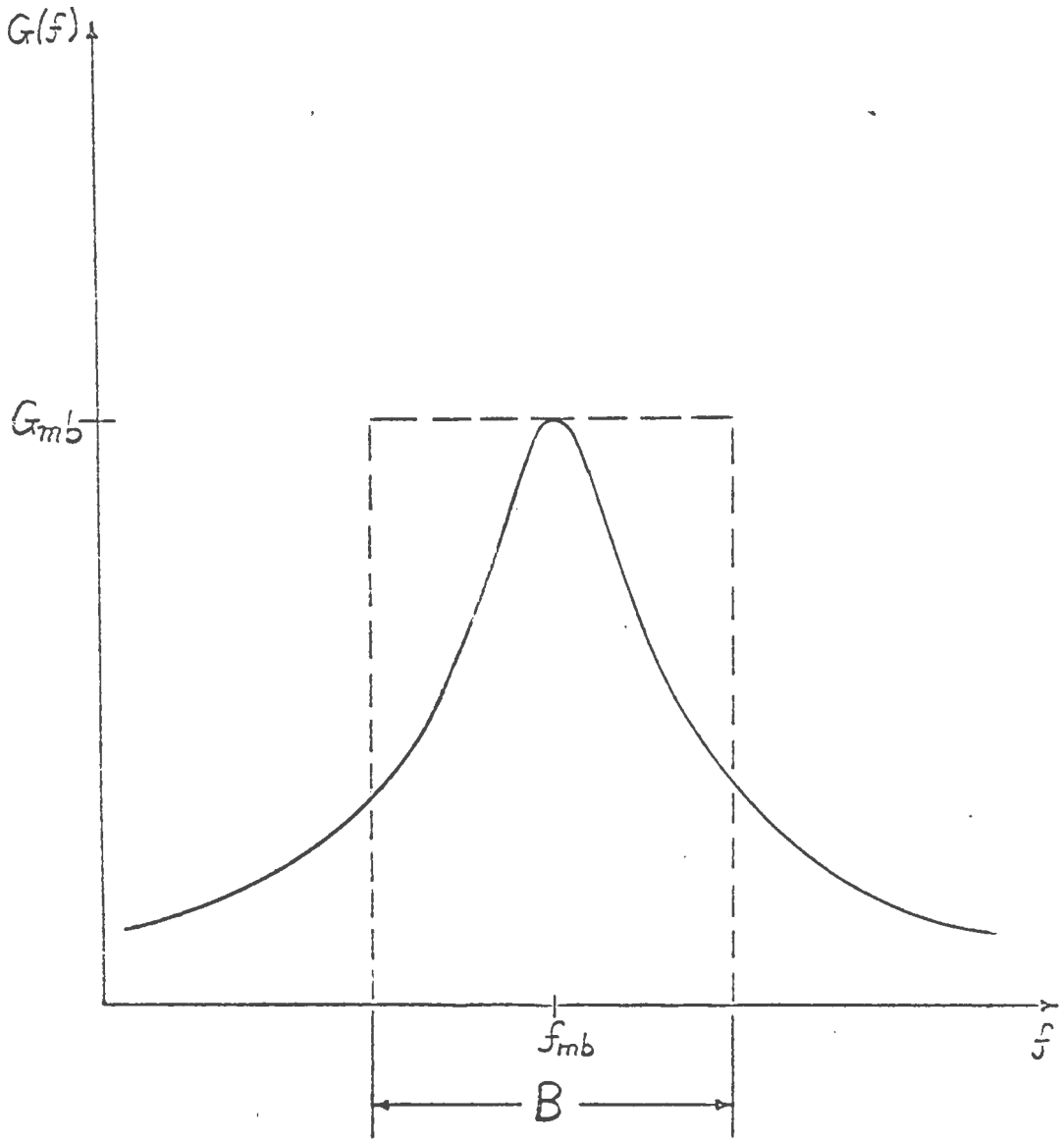

Figure 1. Equivalent noise bandwidth B

$$B = \frac{1}{A_{mb}^2} \int_0^\infty A^2(f)\, df \qquad (3)$$

where the A denotes network voltage gain.

Equation 3 is more useful in obtaining a value for B than Equation 2. If the network equations are unknown or complicated, B may be approximated by plotting the amplifier voltage gain squared versus frequency and constructing a rectangle as shown in Figure 1, whose area approximates the area under the voltage gain squared curve. The most convenient way to approximate the area under the curve is to make the plot on linear graph paper and count the squares. For an extremely narrow-band amplifier whose "skirts" fall rapidly, B is approximately the 3 db bandwidth. For broadband amplifiers having a 6 db/octave roll-off, the noise bandwidth is approximately 1.5 times the 3 db bandwidth.

Johnson noise is an important factor in resistances which are placed in an amplifier circuit at extremely low signal level points. It may also be an important noise contributor in the input amplifying device; however, the circuit designer has no control over device characteristics.

Other random noise sources which exist in the input amplifying device will be briefly discussed later (see Field Effect Transistors).

Low Noise Amplifiers

A low noise amplifier is an amplifier in which special care has been exercised to minimize the noise sources discussed in the previous section.

The 60 cps pickup problem can be minimized by shielding the input circuit. Effective shielding can be achieved by the use of a single conductor cable with a braided metallic shield for the amplifier input lead, and by completely enclosing the low level section of the amplifier. However, when dealing with an amplifier of nano-volt sensitivity, shielding alone is not a satisfactory solution. Such an amplifier can easily be saturated by 60 cps pickup and thus be useless as an amplifier for any frequency. If the desired operating frequency is 60 cps, shielding offers the only hope for success. If the operating frequency is other than 60 cps, frequency selective filters offer the best solution. If the system allows the circuit designer to choose the center frequency of the amplifier, i.e. the frequency of maximum voltage gain, 60 cps should be the last choice. The following two approaches are possibilities for using frequency selective filters to eliminate 60 cps pickup problems. First, a notch filter designed to reject 60 cps can be inserted at the input. This may not be too desirable since additional circuitry might be necessary to provide a low impedance driving source for the filter. Secondly, if feedback is employed, a frequency selective circuit can be placed in the feedback loop to narrow the overall amplifier bandwidth and thus exclude 60 cps from the bandpass. In general, an approach is needed which causes the <u>overall</u> amplifier gain at 60 cps to be very low. A 60 cps rejection filter in a latter stage of the amplifier

would not be effective since the preceding stages could still be saturated by 60 cps pickup.

In many applications, one of the most important specifications on a low noise amplifier is its 60 cps rejection capability. A common method of defining this capability is to specify the following rejection figure:

$$R = 20 \log_{10} \frac{A_{cf}}{A_{60}} \tag{4}$$

where A_{cf} = voltage gain at the center frequency

A_{60} = voltage gain at 60 cps

Experience has indicated that the above rejection figure should be 50 db or better for a good low noise narrow-band amplifier.

Random noise performance of amplifiers can be specified in many ways. For example, one can specify the amplifier's noise figure, or an effective noise voltage referred to the input. In many cases, the specification of noise performance of an amplifier is as nebulous as the sources which cause the noise. Commercial specification writers often go wild in their attempts to specify noise performance. To illustrate this point, we consider three examples of noise performance specifications taken from commercial specification sheets and literature.

1. "Noise figure can be less than 1db."

2. "Input Noise (with input shorted): Less than one nanovolt (10^{-9}v) peak-to-peak (2×10^{-10} volt rms) @ 94 cps."

3. "A signal 40 db below ambient white noise in a 1 Kc bandwidth centered about signal frequency may be recovered with signal to noise ratio of 1."

These different ways of specifying amplifier noise performance present quite a challenge to an individual trying to evaluate amplifiers according to his needs.

Noise figure, probably the most popular way of specifying noise performance, is a method of comparing the noise quality of amplifiers which are operating from the same source resistance in the same frequency range. It is important to remember that the noise figure is meaningless as a method of comparison unless the above conditions are satisfied.

The noise factor F is defined as the ratio of the total output noise power in the amplifier load to the noise power at the output due to the thermal noise of the source resistance. The noise factor can be expressed in terms of voltages as follows:

$$F = \frac{E_{no}^2}{A_n^2 E_{ns}^2}$$

where E_{no} = Total output noise voltage (rms)

E_{ns} = Johnson noise voltage of the source (rms)

A_n = Amplifier voltage gain

The noise figure NF is defined as:

$$NF\ (db) = 10 \log_{10} F$$

$$= 20 \log_{10} \frac{E_{no}}{A_n E_{ns}}$$

Using Equation 1 to express E_{ns} yields:

$$NF\ (db) = 20 \log_{10} \frac{E_{no}}{A_n \cdot 1.28 \cdot 10^{-10} (R_s B)^{\frac{1}{2}}} \qquad (5)$$

The total output noise E_{no} is made up of the noise generated by the source resistance (R_s) and the amplifier itself. Since these two noise sources are completely uncorrelated, they must be combined as a true root-mean-square.

$$E_{no} = A_n \left[E_{ns}^2 + E_{na}^2 \right]^{\frac{1}{2}} \qquad (6)$$

Where E_{ns} = noise due to the source resistance

E_{na} = noise due to the amplifier

For the ideal noise-less amplifier ($E_{na} = 0$), the noise factor becomes one and the noise figure becomes zero db.

Thus it is seen that in order to compare noise figures, the same source resistance must be involved because the noise figure is a function of source resistance. Different noise bandwidths can be involved in the comparison since changing B affects both the numerator and denominator of the noise figure equally.

Another popular way of specifying noise performance is to quote an

effective noise voltage referred to the input with the input shorted. For this figure to be meaningful the frequency at which it was determined must be specified. An advantage of this method is that the source resistance is not involved as in the noise figure. This effective amplifier noise is the quantity E_{na} in Equation 6, so given the source resistance and noise bandwidth of the amplifier, the noise figure can be computed. The value of E_{na} is measured simply by measuring the gain of the amplifier and the noise output voltage with the input shorted and then taking the ratio of the two. This figure gives the absolute sensitivity of the amplifier assuming the noise of the source is small with respect to E_{na}, which is normally true for source resistances below approximately 100 K ohms. Thus the effective input noise approach gives an estimation of the minimum detectable signal of an amplifier.

With the above information at our disposal, we should be able to analyze the example specifications given previously. We recall that the first example stated that the "noise figure can be less than 1 db". This figure indicates that the amplifier is fairly good when compared with the ideal noise-less amplifier (0 db). This conclusion requires a knowledge of what can practically be achieved. However, it tells us nothing about the absolute sensitivity of the amplifier. Since the source resistance and noise bandwidth for which the noise figure was computed are not given, we cannot calculate the effective noise voltage. For example, an amplifier with a 1 db noise figure measured with R_s = 100,000 ohms will generate about 10 times more noise than an amplifier with a 1 db noise figure measured with R_s = 1000 ohms.

The second example quoted a shorted input noise voltage. This is in good form for determining the sensitivity of the amplifier. It is not possible to compute a noise figure because we don't know the noise bandwidth of the amplifier.

The third example presents the biggest challenge of the three. The author of the specification uses "ambient white noise in a 1 Kc band" as a reference voltage. If a resistance were given, we could compute a noise voltage from Equation 1, assuming ambient refers to room temperature, since B is given as 1 Kc. One could then calculate the value of noise voltage which is 40 db below the white noise (or Johnson noise) just calculated. Since the signal to noise ratio for such a signal is given as 1, that is the effective input noise of the amplifier.

We now present the factors which the design engineer must consider in attempting to minimize random amplifier noise. It is advantageous to limit the noise problems to the input stage of the amplifier. The noise generated by succeeding stages of the amplifier can be insignificant if the power gain of the first stage is sufficient. Insight into what constitutes sufficient gain can be obtained from the following equation, called Friis' formula, which relates amplifier noise factor to individual stage noise factors.

$$F_a = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_2 - 1}{G_1 G_2} \qquad (7)$$

where F_a = noise factor of the amplifier

F_1, F_2 = noise factors of first and second stages

G_1, G_2 = power gains of first and second stages

This expression is valid only if all stages have the same noise bandwidth. In most cases the third term of Equation 7 makes no significant contribution so that F_a becomes:

$$F_a = F_1 + \frac{F_2 - 1}{G_1} \tag{8}$$

We want to determine G_1 such that

$$F_a \approx F_1 \tag{9}$$

For Equation 9 to be true, it is sufficient that

$$\frac{F_2 - 1}{G_1} = 0.1\, F_1$$

Solving for G_1

$$G_1 = \frac{F_2 - 1}{0.1\, F_1}$$

or

$$G_1 = \frac{P_o}{P_i} = \frac{E_o^2/R_o}{E_i^2/R_i} = \frac{F_2 - 1}{0.1\, F_1} \tag{10}$$

A less exact but more simplified approach can be followed through the use of effective noise voltages. The effective noise voltages of the first (E_{n1}) and second (E_{n2}) stages can be measured since they are independent of the gain of the stage. In order that the noise of the second stage be

insignificant it is simply necessary that $E_{n1} \cdot A_{v1} = 10\ E_{n2}$ where A_{v1} is the voltage gain of the first stage. Experience has shown this approach to be quite satisfactory.

We can now confine our analysis to the design of the input stage of the amplifier. In most cases the largest noise contributor in the input stage of an amplifier is the active amplifying device. The circuit designer has two factors which he can control. First, the choice of the amplifying device to be used, and second, the electrical operating point of the device. In choosing a transistor for use in the input stage of a low noise amplifier, the designer must determine what noise factors can be expected from a given transistor and what compromises must be made with respect to other types of circuit performance to obtain the desired noise results. Since noise specifications on commercial transistors are sometimes difficult to compare, actual noise measurements may be necessary in order to make the final choice. After the input device is chosen, the designer must obtain data relating the collector current, collector-emitter voltage and the noise factor. The operating point is then chosen for optimum noise factor assuming other circuit performance such as voltage gain and input impedance are not adversely affected. For a given circuit configuration, once the designer has chosen the lowest noise device available and optimized its operating point, there are no other means for reducing the input noise generated. The resistors associated with the input transistor rarely contribute significantly to the overall noise. Resistors in the base circuit should be limited ($<$ 1 megohm) but the other resistors will not normally be significant noise contributors. Low noise wire-wound resistors can be used at lower frequen-

cies if there is any doubt.

At this point, we have theoretically minimized the noise generated by the input stage and thus by the amplifier. This noise is wide-band or flat noise containing components of all frequencies. The amplifier resolution is actually limited by the amount of the wide-band input noise which appears at the output thus masking the desired signal. We can reduce the noise at the output by restricting the frequency response of the amplifier. The system performance may limit how much we can restrict the response. If the amplifier is used to detect a signal of a single frequency, the amplifier bandwidth can be as narrow as possible. The oscillator originating the desired signal would then have to be very stable in order to remain in the passband of the amplifier. Since narrow-band amplifiers are a large class in themselves, the following section is devoted to techniques of narrow-banding.

Narrow-Band Amplifiers

Narrow-band amplifiers or band-pass amplifiers are devices whose frequency response characteristics are determined by a resonant LC or RC circuit. The objective is to pass a single frequency or a small band of frequencies with high voltage gain and provide very little gain for frequencies outside the band. The frequency at which maximum gain occurs is called the center frequency. The bandwidth is the familiar 3 db bandwidth, the difference between the frequencies at which the gain is 0.707 times the gain at the center frequency.

For relatively high frequency amplifiers, resonant LC circuits are placed in the base and collector circuits to provide the spectrum-shaping properties of the amplifier. The resultant bandwidth is dependant on the sharpness of the tuned circuit and the loading on it. The more a tuned circuit is loaded, the broader its frequency characteristic becomes. At lower frequencies, especially below 1000 cps, LC circuits become difficult to work with because of the large capacities required. For example, the large capacities make it difficult to conveniently "trim" the filter to adjust its center frequency to that of an oscillator providing the signal to be amplified. RC filters are generally more desirable for use at lower frequencies. A type of RC filter which is suitable for use at frequencies up to several Kc is the parallel-T filter. Since the parallel-T filter has been chosen for use in the design example, a following section is devoted to its explanation. Figure 2 shows a special type of narrow-band feedback amplifier using the parallel-T filter in the feedback loop. At the center frequency of the amplifier there is theoretically no negative feedback, thus high gain. For frequencies other than the center frequency there is negative feedback, thus very little amplifier gain. The amplifier A is a conventional wideband transistor amplifier. The adder is restricted only by the requirement that it provide a high impedance load for the filter. A more detailed analysis of this type amplifier is presented in a later section of this report.

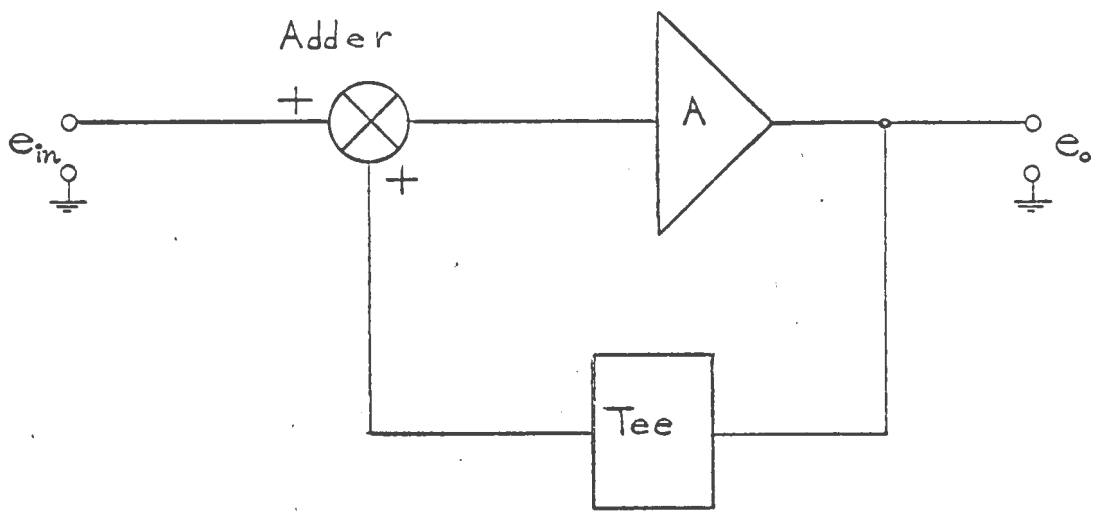

Figure 2. Parallel-tee feedback amplifier

Field Effect Transistor

The device chosen for the first stage of amplification in the proposed narrow-band amplifier is the field effect transistor. A field effect transistor (FET) is essentially a semiconductor current path whose resistance is modulated by the application of an electric field perpendicular to the current (2). This modulating field results from the reverse biasing of a P-N junction. The electrical characteristics of the FET are similar to those of a pentode vacuum tube.

There are two types of FET's, P-channel and N-channel which are analagous to PNP and NPN junction transistors. The letter P or N denotes what the majority carrier of the device is, i.e., P for holes and N for electrons. Figure 3 shows a P-type bar of silicon with N-type sections forming P-N junctions. The FET terminal designations and their vacuum tube analogs are: gate-grid, source-cathode, and drain-plate. When a P-N junction is reverse biased a depletion or space-charge layer develops on either side of the junction in which there are no current carriers. When the two P-N junctions are reverse biased the resulting depletion layers effectively reduce the size of the channel through which the majority carriers flow. This means that as the effective channel size is controlled the resistivity of the channel is likewise controlled. Therefore the source-drain resistivity can be modulated by varying the gate-source or gate-drain voltage. The saturation region or pinch-off region is where a further increase in drain-source voltage results in very little change in drain current. Figure 4 shows a characteristic experimentally determined for a 2N2386.

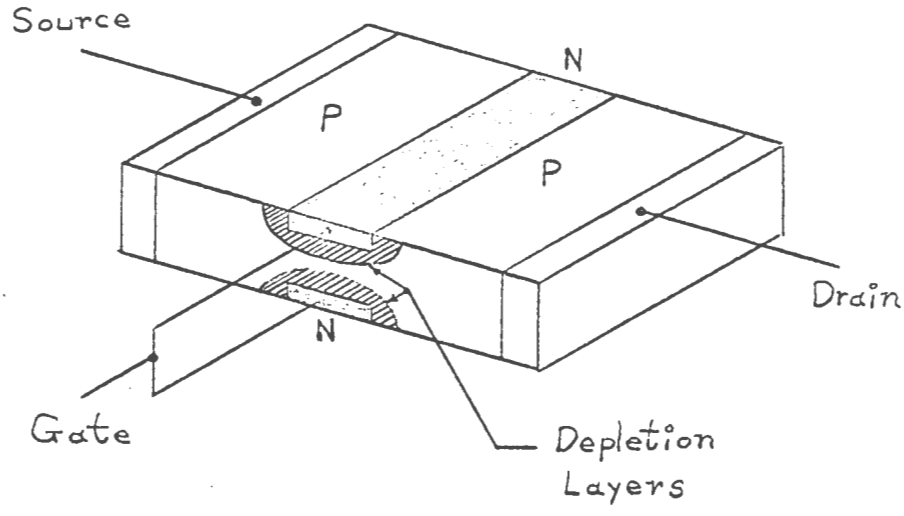

Figure 3. FET construction

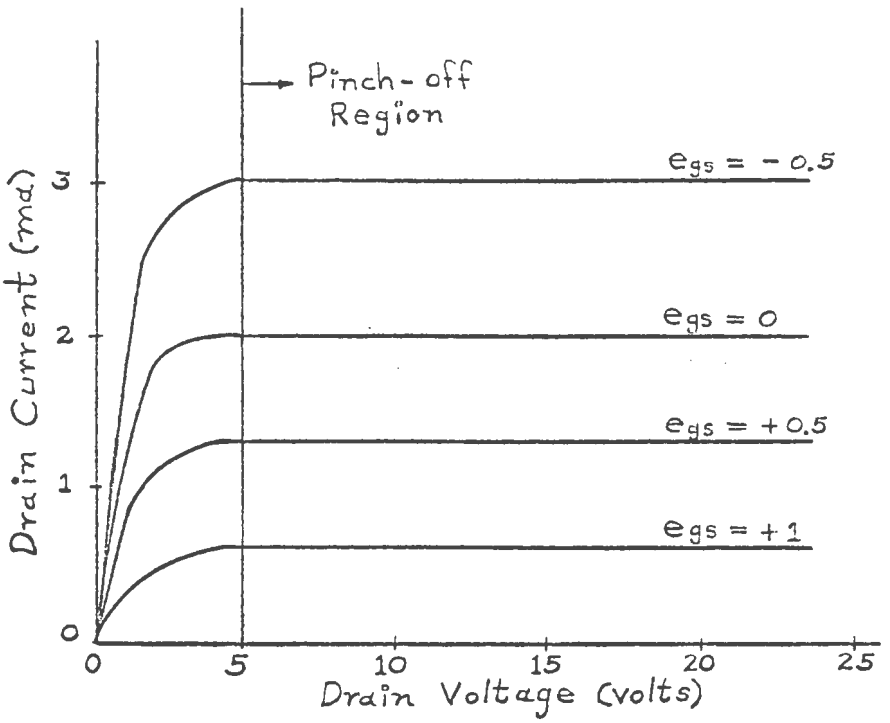

Figure 4. 2N2386 drain characteristics

The primary disadvantage of ordinary junction transistors is the difficulty of designing an amplifier circuit having a high input impedance, say several megohms. Vacuum tubes provide this capability but have the disadvantage of having a filament and microphonic noise. The FET embodies the advantages of the transistor and the vacuum tube without many of the disadvantages. A simple amplifier circuit can be designed having an input impedance of several megohms without any tricky techniques. The FET does have the problem of all transistors that the characteristics are not uniform from one unit to another. For example, a zero biased FET in a particular circuit may yield a drain current of 2 ma and a drain-source voltage of 5 volts. If another FET of the same type is inserted in the circuit the drain current and drain-source voltage may be changed by 100%. Thus one cannot design accurately from data sheets as is the case with vacuum tubes.

The FET compares quite well with the best low noise vacuum tubes for noise generation. The random noise sources in an FET are thermal noise in the conducting channel, shot noise of the gate current, and 1/f noise of the gate and channel currents. The 1/f noise does not become significant until the frequency drops below about 100 cps at low source impedances. For higher source impedances, say 1 megohm, the break occurs at about 1,000 cps.

The random noise generated by a vacuum tube and a junction transistor is a function of the operating point. To optimize the operating point, it is necessary to know exactly how the noise varies with operating point. Tests were made on the 2N2386 FET using the noise measuring system described in Appendix B. Similar tests were performed on two low noise vacuum tubes,

the 6DS4 nuvistor and the 6AC7, to obtain comparative noise performance data. Figures 5, 6, and 7 show the results of these tests.

The tests show that the FET noise is essentially independent of drain-source voltage and increases only for small values of drain current. The 6DS4 noise was greatest at high plate voltages and small plate currents. The 6AC7 noise varied in a manner similar to the 6DS4. It must be remembered that as one approaches zero bias on any of the three devices, the input impedance of the amplifier decreases. Therefore the circuit application might prohibit the designer from optimizing the operating point for low noise.

The noise data shows that the three devices tested are about equal for noise generation. The 6DS4 appears to be potentially best for low input impedance applications. The input impedance for the lowest noise point for the 6DS4 was approximately 400 K ohms. The 6AC7 was extremely bad for microphonic noise.

Parallel Tee Filter

The parallel tee filter is the heart of the proposed low noise narrow-band amplifier. The shape of the amplifier response will be essentially that of the parallel-tee filter. Thus the effective Q of the amplifier will be determined by the Q of the filter.

The parallel tee filter circuit is shown in Figure 8. It is essentially a low pass filter in parallel with a high pass filter whose composite characteristic is that of a notch filter. The transfer function can be represented by the following expression:

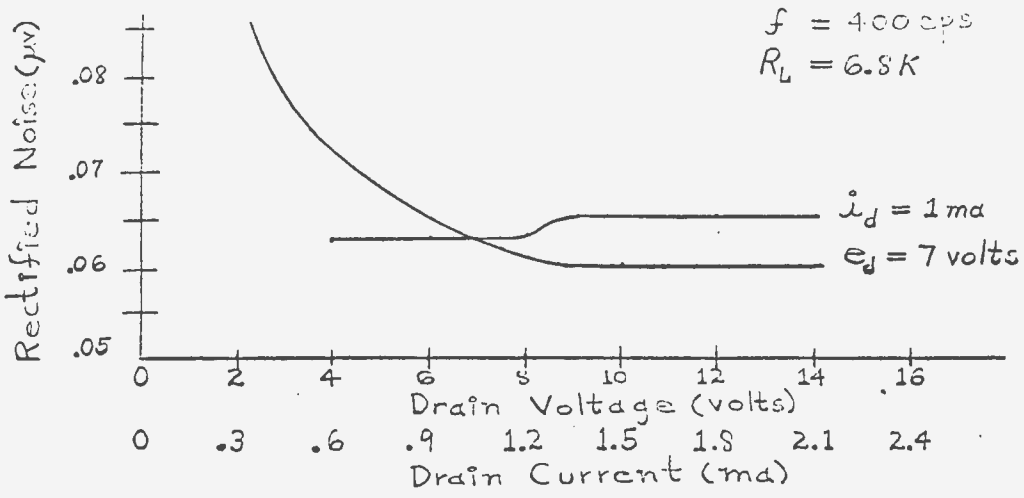

Figure 5. 2N2386 noise characteristics

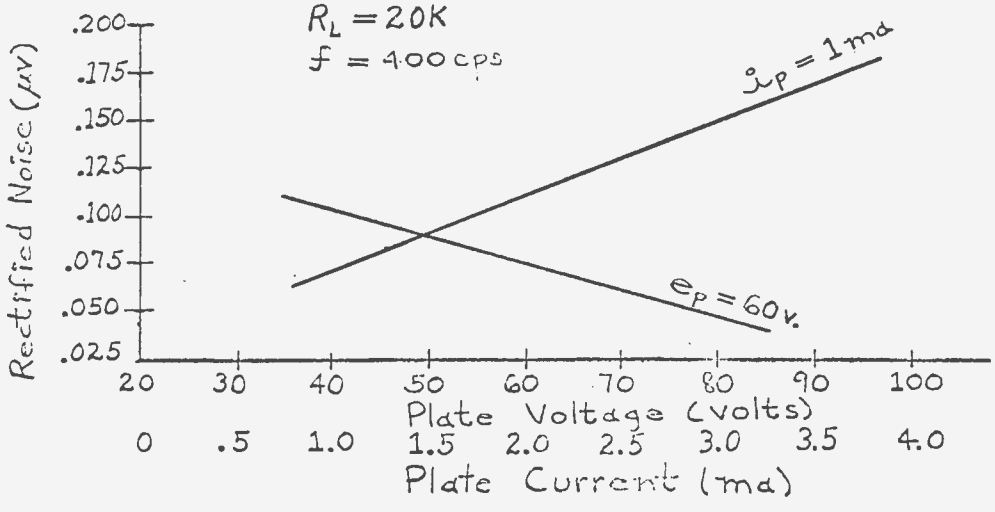

Figure 6. 6DS4 noise characteristics

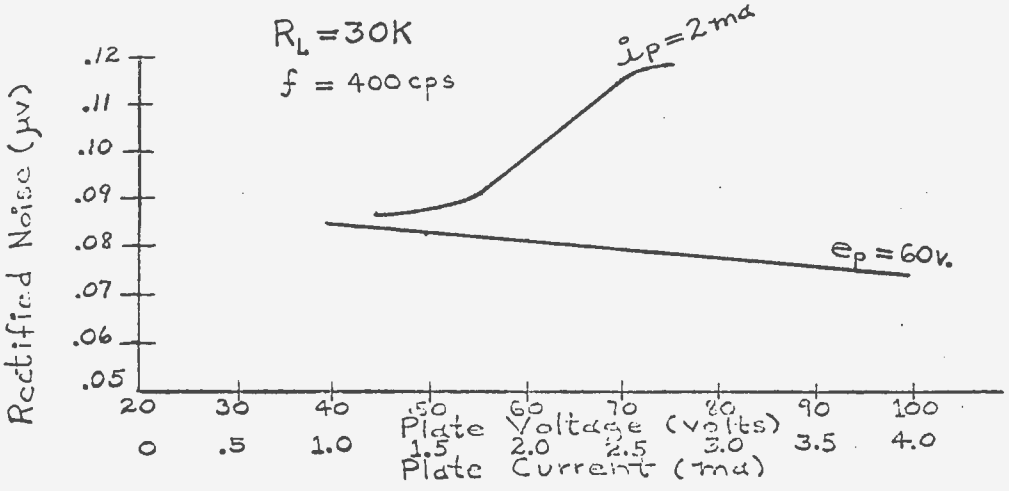

Figure 7. 6AC7 noise characteristics

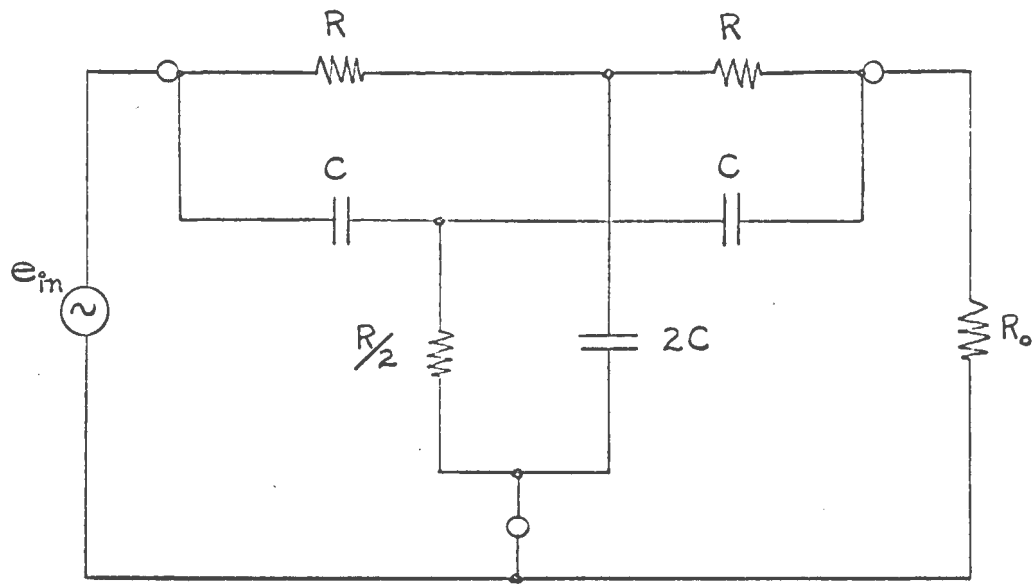

Figure 8. Parallel-tee filter circuit

$$\frac{e_o}{e_{in}} = \frac{R_o \left[1 - \omega^2 C^2 R^2\right]}{\left[R_o(1 - \omega^2 C^2 R^2) + 2R\right] - j \left[2 \omega CR (R + 2R_o)\right]} \qquad (11)$$

where R_o = twin-tee load resistance

C, R = components of the tee

The derivation of this equation (see Appendix A) was made under the following assumptions:

a. The twin-tee is driven by a zero impedance source.

b. The tee is assumed to be symmetrical which is the narrow-band case.

It will be shown later that the zero source impedance assumption does not affect the usefulness of the equation in practical situations. The equation shows that there is a single frequency at which there is theoretically infinite rejection. The condition for infinite rejection is:

$$\omega_o^2 C^2 R^2 = 1$$

$$\omega_o = \frac{1}{CR}$$

$$f_o = \frac{1}{2 \pi CR} \qquad (12)$$

where f_o = the center frequency

The design of a twin-tee filter is begun by choosing a value for R in the filter. It has been shown in the literature (3) that R should be chosen according to:

$$R = \left[2 R_1 R_o\right]^{\frac{1}{2}} \qquad (13)$$

where R_1 = resistance of the driving source

R_o = resistance of the load

Experience indicates that this relation can be looked at as a lower limit for R. Although the literature defines Equation 13 to be the narrow-band case, choice of higher values for R does not affect the bandwidth assuming the load impedance is high, say $\geq$ 1 megohm. The value for C is chosen such that $\frac{1}{\omega C} = R$ at the desired center frequency. In order to obtain a high Q, it is very important that the filter be symmetrical. Best results are obtained if the resistors and capacitors are measured and matched on an impedance bridge.

The most significant factor which might cause broadening of the tee response is the load R_o. The more the tee is loaded, the broader its response becomes. This can be shown by calculation using Equation 11 or more conveniently by experimentation. Tests were performed on a sample tee to study the effects of loading on its response and to verify the validity of Equation 11. The circuit tested is shown in Figure 9. The circuit is designed for a center frequency of 398 cps. The unusual center frequency resulted from the choice of standard value capacitors. Figure 10 shows the variation of voltage transfer and phase with frequency for different values of load. This dramatically shows the broadening affect of a reduction in the tee load resistance. The theoretical curve obtained from Equation 11 for R_o = 1 megohm is shown dotted in each plot, and is shown to agree closely.

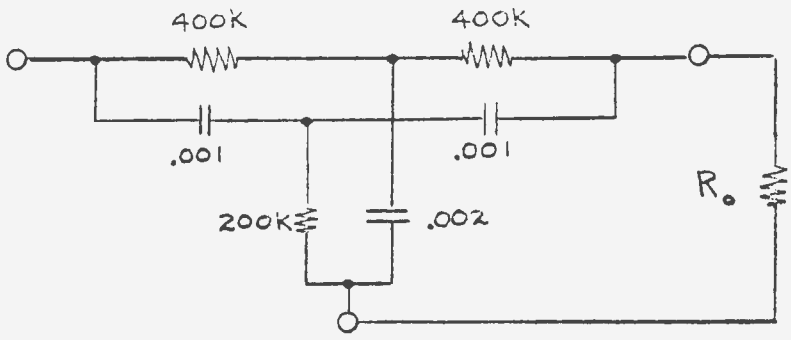

Figure 9. 398 cps parallel-tee filter

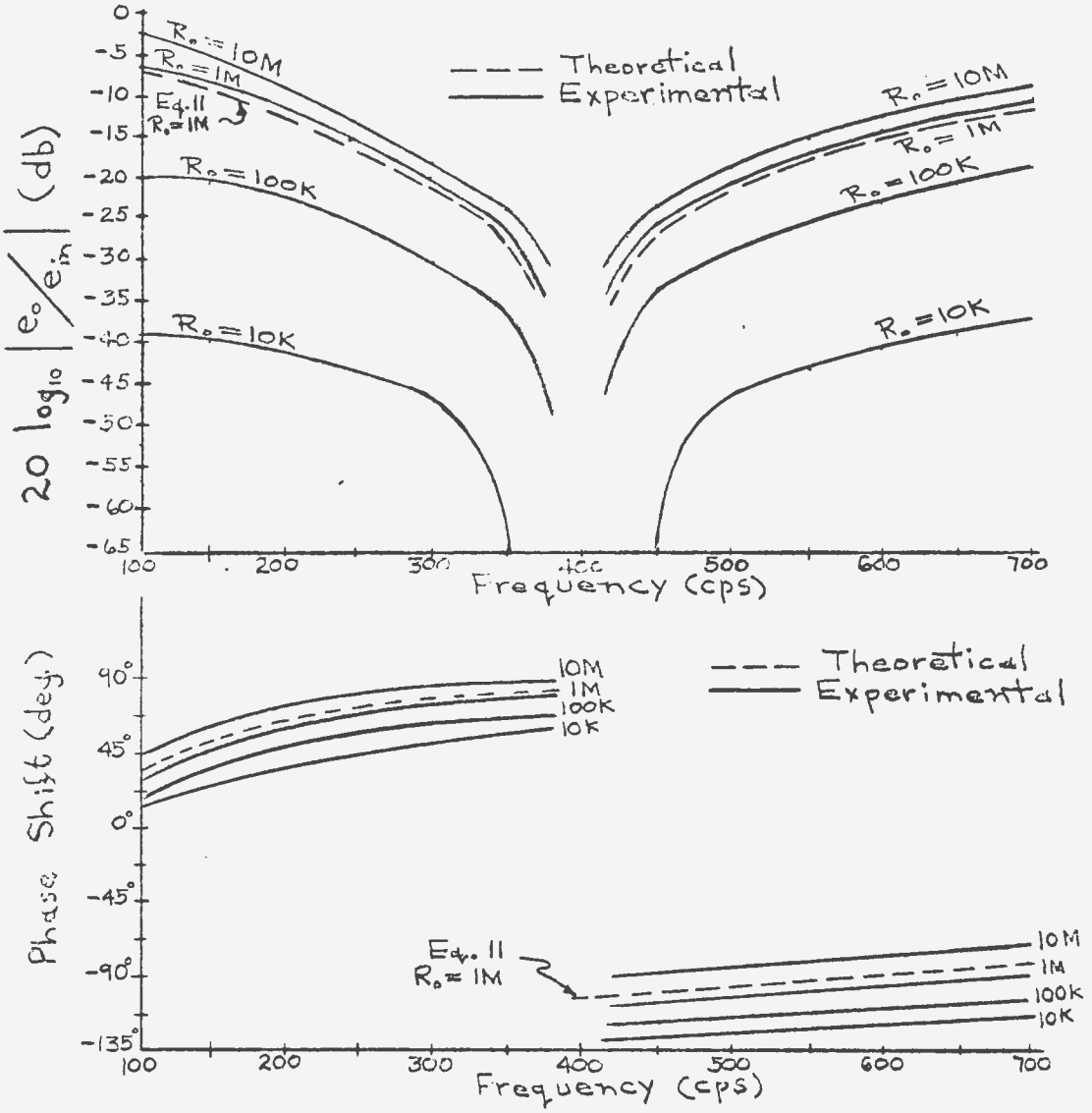

Figure 10. 398 cps filter response curves

The test tee was driven from a 600 ohm source impedance. The input impedance of the tee was measured to be approximately 300 K ohms in the region about the center frequency. This would allow source impedances up to about 30 K before causing any significant effects on the response.

The fact that a high impedance load for the tee is desirable will influence the design of the proposed feedback narrow-band amplifier.

PRACTICAL CONSIDERATIONS

Low Noise Narrow-band Amplifier Specifications

With the preceding theoretical considerations in mind, the objective now is to design an improved low noise narrow-band amplifier using field effect transistors. The goal is to achieve an amplifier which will form the basis for a sensitive AC null detector or a DC micro-voltmeter. The design of such a device will conform to the following specifications:

Center frequency	$\approx$	400 cps
Center frequency gain	--	500
60 cps rejection	$>$	40 db
Input impedance	$\geq$	1 megohm
Microphonics	--	none

The above-mentioned applications of the proposed amplifier are discussed in a later section of this report.

Practical Circuit Design

The design of the low noise narrow-band amplifier begins with the choice of a specific circuit configuration. The scope of this investigation includes the design of the two basic configurations shown in Figure 11. The two circuits differ primarily in the input stage where one has a drain-coupled adder and the other has a cascode adder.

We shall first consider the design of the drain-coupled input circuit. The design procedure begins with a study of the field effect transistor as a voltage amplifier. The simple voltage amplifier circuit is shown in Figure

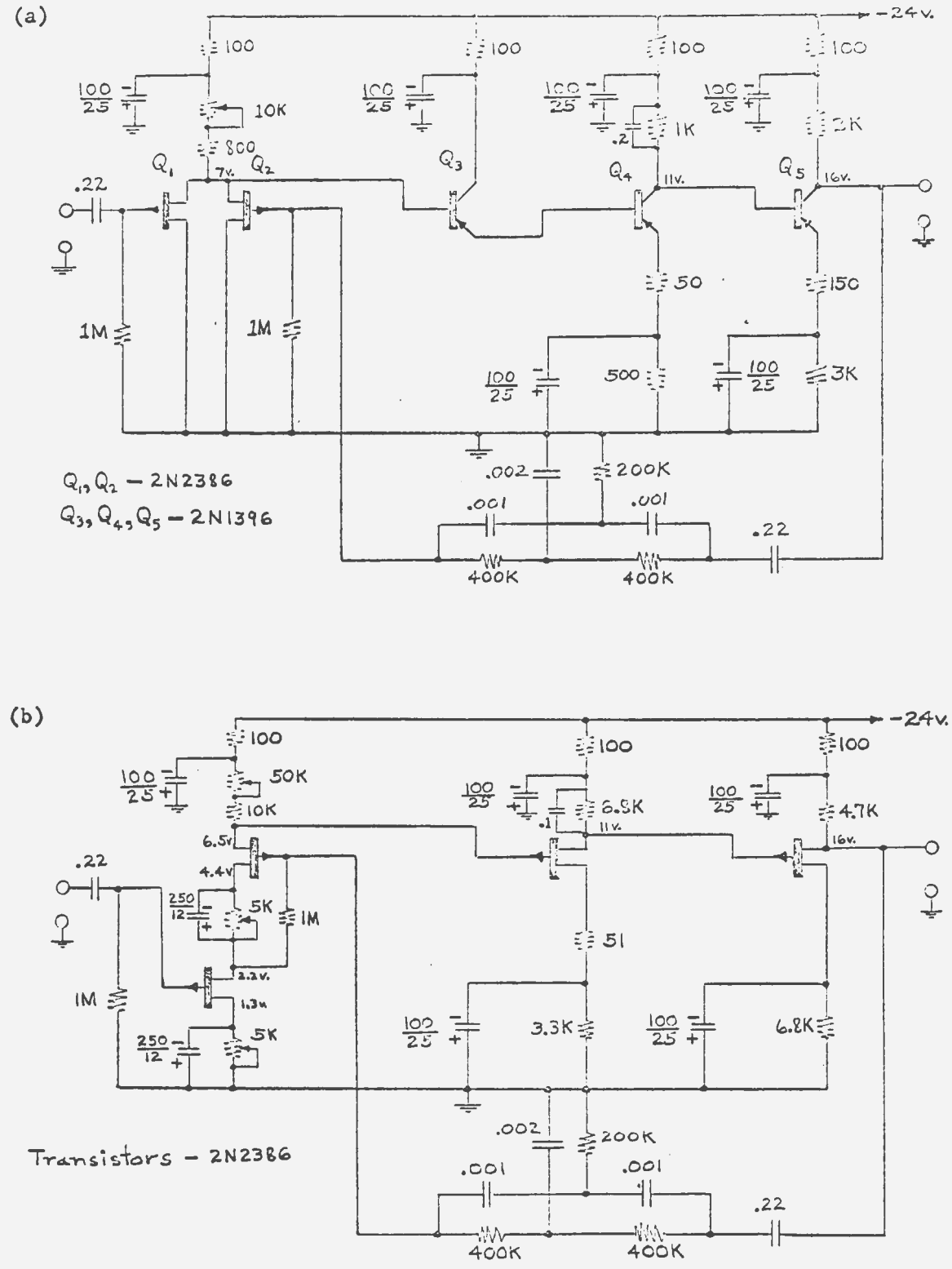

Figure 11. Basic amplifier configurations

12. The voltage gain can be derived from the equivalent circuit shown in Figure 13. Summing the currents at the output node gives

$$g_m e_{in} + e_o g_o + e_o/R_L = 0$$

$$e_o (g_o + 1/R_L) = - g_m e_{in}$$

$$A_v = \frac{e_o}{e_{in}} = \frac{- g_m}{G_o + 1/R_L} = \frac{- g_m R_L}{1 + g_o R_L} \qquad (14)$$

where g_o = output conductance of FET

g_m = transconductance of FET

R_L = load resistance

Typically the product $g_o R_L << 1$, which reduces Equation 14 to

$$A_v = - g_m R_L \qquad (15)$$

The drain characteristics of a 2N2386 FET are shown in Figure 14. The transconductance of an FET is defined as

$$g_m = \frac{\Delta i_d}{\Delta e_g} \Bigg|_{e_d = \text{constant}}$$

To get maximum gain the operating point of the FET must be placed in the pinch-off region where the wide spacing of the curves results in largest possible values of g_m. The g_m remains relatively constant throughout the

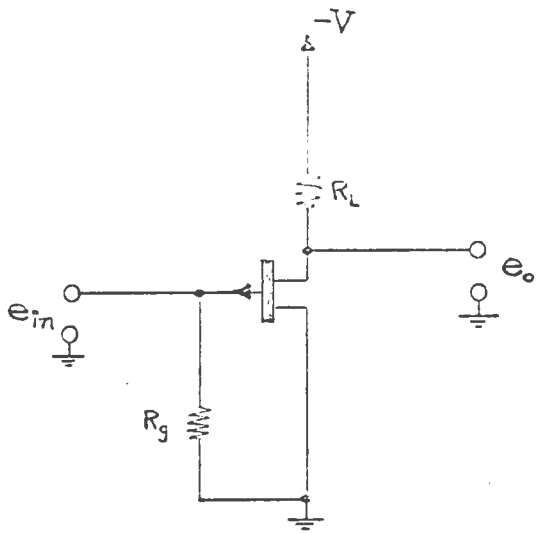

Figure 12. FET voltage amplifier

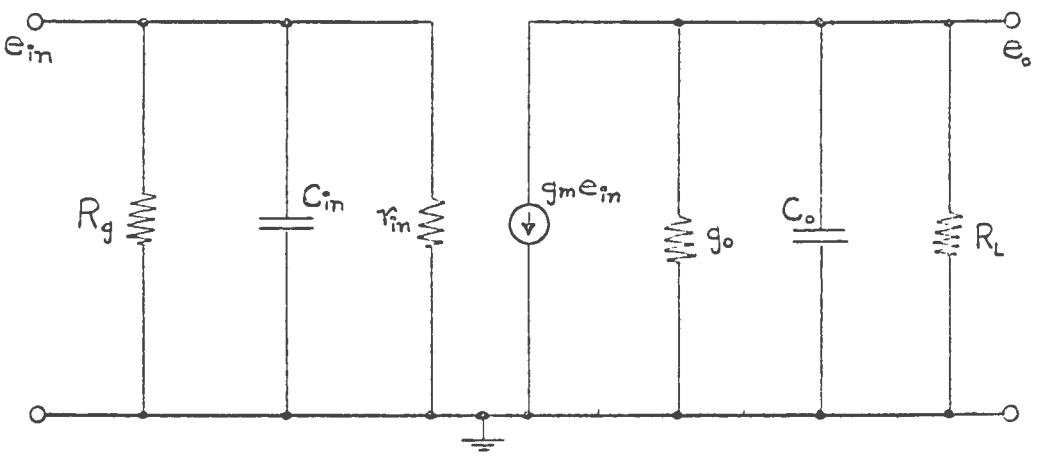

Figure 13. Amplifier equivalent circuit

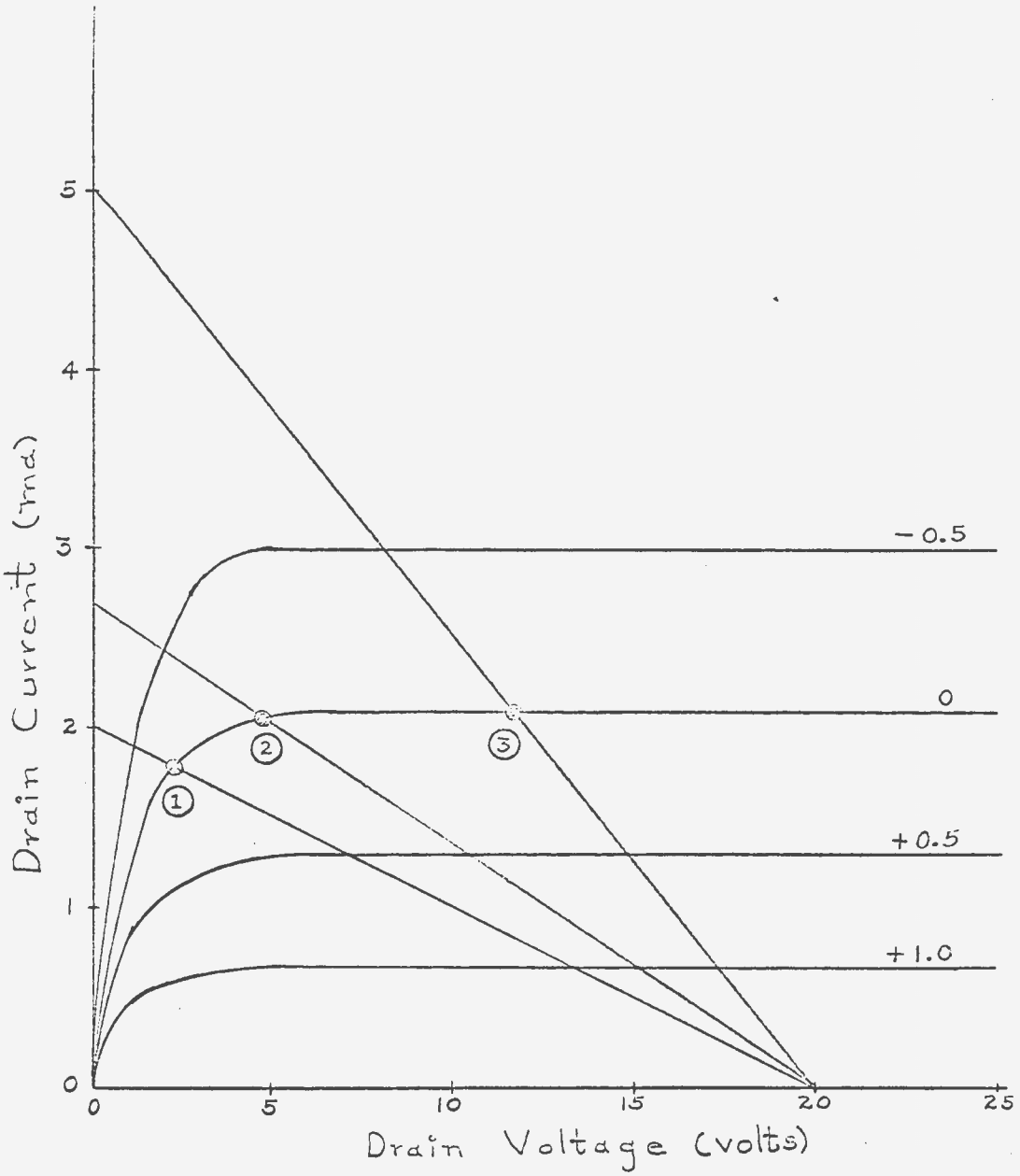

Figure 14. 2N2386 drain characteristics

pinch-off region. Thus for a given e_g maximum gain is obtained by operating at the "knee" of the curve which corresponds to the largest R_L while still maintaining maximum g_m. This point is illustrated by the three sample operating points shown in Figure 14. The gain at the three points can be computed from Equation 15 as:

$$1. \quad A_v = g_m R_L = \frac{(1.9 - 1.3)\ 10^{-3}}{1} \cdot 10\ K = 6$$

$$2. \quad A_v = \frac{(2.5 - 1.3)\ 10^{-3}}{1} \cdot 7.5\ K = 9$$

$$3. \quad A_v = \frac{(3 - 1.3)\ 10^{-3}}{1} \cdot 4\ K = 6.8$$

The actual gain measured for point 2 was 9.5. Thus for operating at zero bias, the best operating point from the standpoint of voltage gain is point 2. However, this is not the only consideration in picking the operating point. The circuits of Figure 11 are direct coupled throughout so that the voltage at the drain is limited. There must be enough voltage left so that the following stages can be operated at a high gain operating point. The desired DC levels were chosen arbitrarily to be those shown in Figure 11a with a power supply voltage of 24 volts, Zener regulated. The junction transistors must have 4 or 5 volts from collector to emitter in order to obtain sufficient voltage gain and to have a reasonable dynamic range. Thus the input drain voltage is fixed at approximately 7 volts. The gate bias was chosen to be zero even though there are other points which give slightly higher gain. Since FET characteristics are non-uniform from one unit to

another, the drain resistor and the self-biasing source resistors must be determined experimentally for each transistor. Operating at zero bias eliminates the source resistors from this consideration. By placing a variable resistance in the drain circuit, the DC level can be adjusted easily to the FET's being used.

The emitter follower stage provides a high impedance load for the adder. The following two stages are conventional voltage amplifiers with some current feedback in the interest of gain stability and linearity.

Figure 15 shows a variation of the drain-coupled circuit of Figure 11a. The wideband amplifier section uses all field effect transistors instead of junction transistors. The high input impedance FET stages eliminate the need for an emitter follower. The use of a low noise FET following the input stage eases the gain requirements on the input stage. Since the 2N1396 junction transistor is a larger noise contributor than the FET, the input stage gain required to "bury" the noise of the second stage in Figure 11a is beyond the capability of the FET input. Thus the circuit of Figure 15 should yield a better low noise capability than the circuit of Figure 11a. This point will be verified in the section on Circuit Performance.

The cascode input stage is more difficult to design since the operating point of one FET affects the gain of the other. The upper FET acts as part of the load impedance of the lower FET so that the gain of the lower one varies as the operating point (resistivity) of the upper one is changed. The lower FET is actually an unbypassed impedance for the upper one so that as more voltage appears across the lower one, increasing its resistivity, the

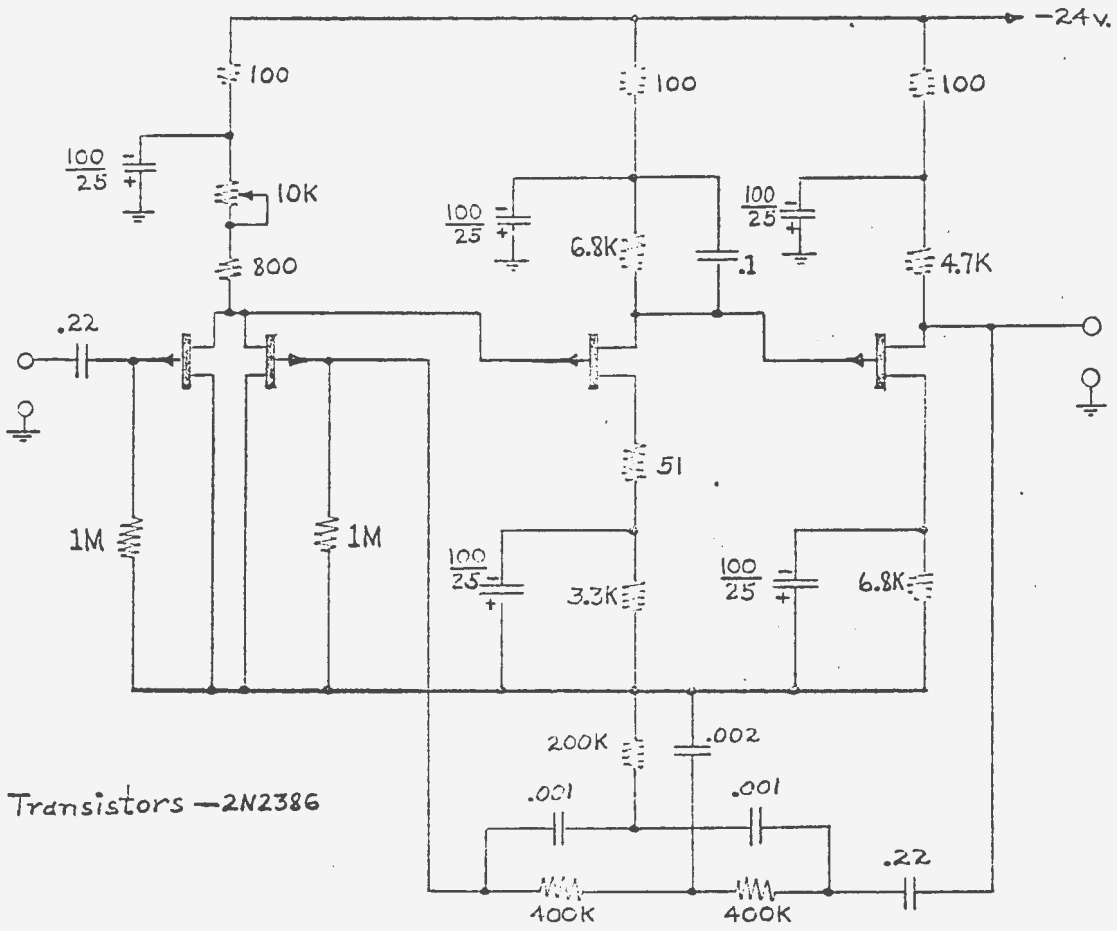

Figure 15. Drain-coupled FET circuit

gain of the upper decreases. For maximum gain of the upper FET, the lower FET must be saturated and therefore useless as an amplifier. Thus by varying the two operating points, one can reduce the gain of one while increasing the gain of the other. Since we want as much signal gain as possible in the input stage, the gain of the signal transistor was chosen to be higher than that of the feedback FET. By using variable resistors for source resistors and drain resistor, the optimum DC levels were found to be those shown in Figure 11b. This resulted in a gain of 12 from the signal terminal to the adder output and a gain of 6 from the feedback terminal. After the resistor values are determined experimentally for the FET's used, the variable resistors can be replaced by fixed resistors.

In both of the above input stages, the load on the parallel tee filter is an important consideration. From previous information, we know that the higher the tee load impedance the higher the Q of the circuit will be. The problem is the choice of the gate return resistor. It should be large so as not to load the filter; however, it is in the input circuit where its Johnson noise could be an important noise factor if it were chosen too large. It was found by experimentation that the optimum value was 1 megohm.

The parallel tee filter used in both amplifiers was the test tee discussed earlier in the section devoted to the filter circuit.

The capacitor which appears across the collector load of the junction transistor amplifier has to do with oscillation and is discussed in the following section.

Oscillation

In designing an amplifier of the type described, oscillation is one of the primary problems encountered. To solve such problems in feedback amplifiers, it is necessary to understand the possible causes of oscillation. A feedback amplifier becomes an oscillator when the feedback signal contains a frequency component for which there is unity loop gain and a 180^{o} phase shift in the loop. Another possible cause of oscillation is high level ground currents passing near the low level input stage. This can be avoided by shielding of the input and by careful placement of ground leads.

The use of direct coupling eliminates the possibility of interstage circuitry introducing phase shifts in the loop which could cause oscillation. The parallel tee filter introduces varying phase shifts depending on the frequency. Since the feedback signal theoretically contains all frequencies, it is quite probable that the phase shift of the loop will be 180^{o} for some frequencies. The result would be oscillation at a frequency other than the center frequency of the amplifier. The actual problem encountered in the design of the amplifiers was oscillation at a high frequency, approximately one megacycle. The most convenient way to solve problems of high frequency oscillation is to further restrict the response of the loop. The voltage transfer of the filter is low at one megacycle but the gain of the wideband stages may offset the filter attenuation enough to cause oscillation. A small capacitor placed in parallel with the collector load of one of the wideband amplifiers reduces the high frequency response of the loop enough to stop the oscillation without appreciably affecting the 400 cps gain. The loop phase shift at one megacycle may still be approximately 180^{o} but oscil-

lation cannot occur without sufficient loop gain.

Oscillations can be caused by signals injected at the input drain by the power supply. The amplifier can be protected from problems of this type by use of RC decoupling networks in each stage.

Another possibility is oscillation at the center frequency of the amplifier. This is normally caused by the fact that the filter is delivering a regenerative signal to the feedback terminal of the adder. This can be easily verified by comparing the open loop gain with the closed loop gain. If the filter is properly nulled, the two gains should be equal. If the closed loop gain is higher, the circuit is regenerative. The variation of the shunt elements in the tee, holding the RC product constant, results in the elimination of the regeneration without causing a shift in the center frequency of the amplifier. This must be achieved by experimentation.

Circuit Performance

The performance characteristics of the three low noise narrow-band amplifiers described are summarized in Table 1. The circuits are designated by the figure numbers of schematics which appear in the Practical Design section. The results indicate that the cascode input circuit achieves the lowest noise of the three circuits. For applications where absolute sensitivity is the main objective, the cascode circuit is preferred. In applications where frequency selectivity is most important, the circuit of Figure 11a is preferred because of its extremely high Q of 190.

The response curves of the three amplifiers are identical in shape with

the only difference being in the width of the bandpass. Figure 16 shows the response curves for the circuit of Figure 11a. The curves show the effect of changing the value of the feedback gate return resistor which directly loads the parallel tee filter. The curves clearly show the importance of not loading the filter circuit.

Table 1. Circuit performance

CIRCUIT	GAIN	Q	INPUT NOISE (RMS)	60 cps REJECTION	CENTER FREQUENCY
Figure 11a	600	190	0.5 μv	51 db	399.6
Figure 11b	1,400	20	0.28 μv	38 db	392.5
Figure 15	350	78	0.38 μv	44 db	396.0

The input impedance of the amplifiers was determined by the gate return resistor which was 1 megohm.

The exact configuration of the three resultant amplifiers is workable up to approximately 20 Kc. At higher frequencies LC circuits can be used as the frequency selective circuit.

Mechanical Considerations

The construction of low level circuits is generally a critical operation. Enemies of such circuits which arise in the construction are chassis

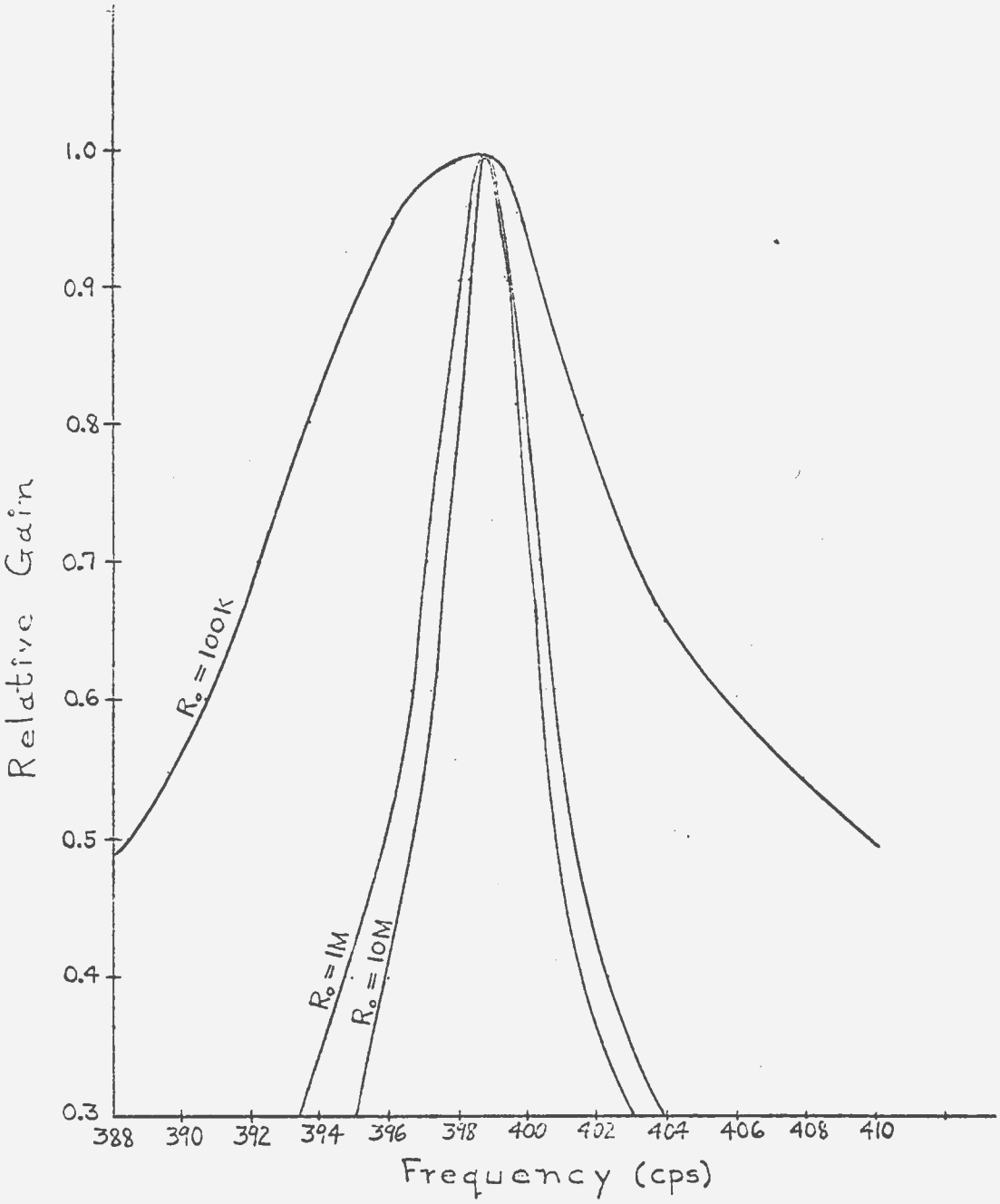

Figure 16. Parallel-tee amplifier response

ground currents, ground loops, and pick-up from one stage to another. It is extremely important that the input stage be electrostatically shielded from external fields and from other high signal level points in the circuit. In vacuum tube circuitry of this type, there must be only one chassis ground in order to prevent ground currents from circulating in the chassis and causing pickup at the input circuit. The use of printed circuit cards in solid state circuitry eliminates problems of this type to a great extent.

PARALLEL TEE AMPLIFIER ANALYSIS

A detailed mathematical analysis of the parallel tee feedback amplifier is beyond the scope of this investigation. The purpose of this section is to present insight for making such an analysis. The presence of the parallel tee filter in the feedback loop greatly complicates the analysis of the amplifier. A block diagram representation of the three amplifiers described is shown in Figure 17. The transfer functions shown are defined as follows:

K_s = gain from signal terminal to adder output

K_f = gain from feedback terminal to adder output

K_w = gain of wideband amplifier stages

K_t = transfer function of parallel tee filter

The output voltage e_o can be expressed by the following equation:

$$e_o = K_w \left[K_s e_{in} + K_f K_t e_o \right]$$

which yields

$$\frac{e_o}{e_{in}} = \frac{K_w K_s}{1 - K_w K_f K_t} \tag{16}$$

From this equation the response characteristics of the three amplifiers described could be computed. The complex expression for K_t is given by Equation 11. While Equation 16 can completely describe the characteristics of the parallel tee feedback amplifier, the time consumed in making such calculations inevitably drives one to the laboratory bench and the soldering iron.

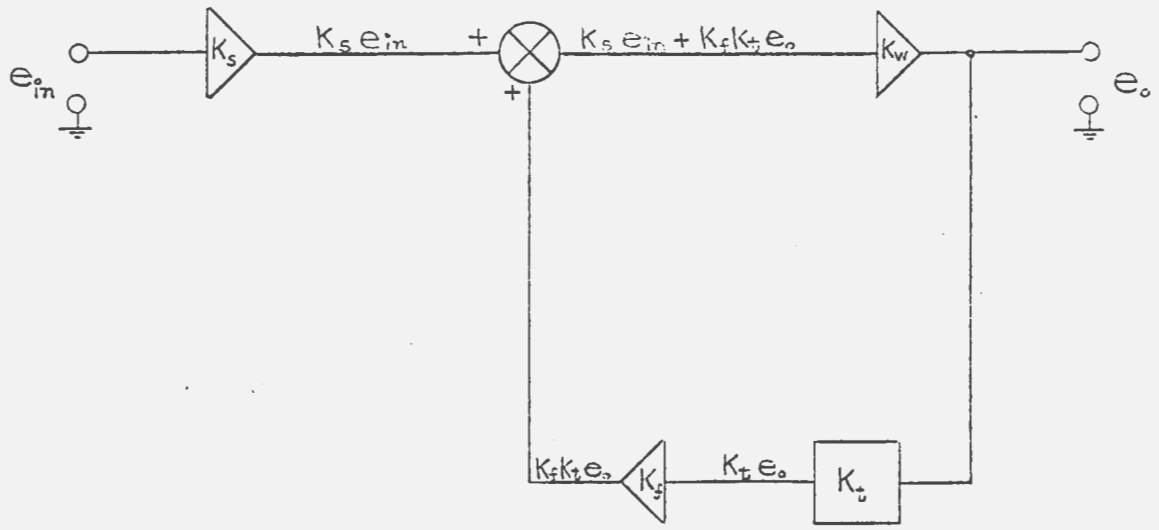

Figure 17. Block diagram of amplifiers

APPLICATIONS

The resultant low noise narrow-band amplifiers find application in many systems which require frequency selective amplification. Two applications of such an amplifier are as a phase-lock detector (4) and as a DC carrier-type micro-voltmeter.

The phase-lock detector is used as a null detector for precision balancing of AC Kelvin bridges. The detector would consist of two stages of narrow-band amplification whose output is delivered to a phase discriminator circuit. The addition of the phase discriminator circuit further increases the overall Q of the circuit thus permitting an even lower least detectable signal. A sensitivity of the order of 30 nano-volts RMS is normally possible.

The addition of a low noise mechanical chopper and associated circuitry at the input of the phase-lock detector yields a DC carrier-type amplifier. The chopper and discriminator are operated at the center frequency of the narrow-band amplifier. The sensitivity is limited by the noise characteristics of the chopper and the amplifier. Instability due to thermally generated potentials in the chopper input circuit is usually the primary design problem. A full-scale sensitivity of the order of 0.01 microvolt DC is normally possible.

CONCLUSIONS AND SUMMARY

The objective of designing an improved solid state low noise narrow-band amplifier is achieved in the amplifiers described in this report. The field effect transistor is an input device whose noise characteristics are comparable to the better low noise vacuum tubes. The high input impedance allows simplified solid state circuitry to result in impedance levels of the order encountered in vacuum tube circuitry. The problem of microphonic noise is completely eliminated. A simple Zener regulated power supply replaces the feedback regulated filament supply and plate supply needed in vacuum tube circuitry. This greatly reduces the cost of the improved amplifier as compared to the tube amplifier. The time required in the construction of the solid state amplifier is about one-half that required for the tube circuitry. This represents a further reduction in the overall cost of the "black box" which will provide low noise narrow-band amplification.

The FET cascode input circuit achieved the best effective input noise which was measured at 0.28 μv RMS. The drain-coupled input circuit followed by conventional junction transistors resulted in a circuit Q approaching 200 at a center frequency of 400 cps.

The conclusion is that the FET is an excellent solid state device for use in low noise applications.

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APPENDIX A

Derivation of Parallel Tee Filter Transfer Function

The derivation of the transfer function of the parallel tee filter is based on the symmetrical tee circuit shown in Figure 18. The tee components are expressed in terms of admittances in order to be suitable for a nodal analysis. The three node voltage equations are:

$$-\left[2Y_5 + 2Y_3\right] e_1 + \left[0\right] e_2 + \left[Y_5\right] e_o = -Y_5 e_{in}$$

$$\left[Y_5\right] e_1 + \left[Y_3\right] e_2 - \left[Y_o + Y_3 + Y_5\right] e_o = 0$$

$$\left[0\right] e_1 - \left[2Y_3 + 2Y_5\right] e_2 + \left[Y_3\right] e_o = -Y_3 e_{in}$$

The determinant denominator Δ is:

$$\Delta = \begin{vmatrix} -\left[2Y_5 - 2Y_3\right] & \left[0\right] & \left[Y_5\right] \\ \left[Y_5\right] & \left[Y_3\right] & -\left[Y_o + Y_3 + Y_5\right] \\ \left[0\right] & -\left[2Y_3 + 2Y_5\right] & \left[Y_3\right] \end{vmatrix}$$

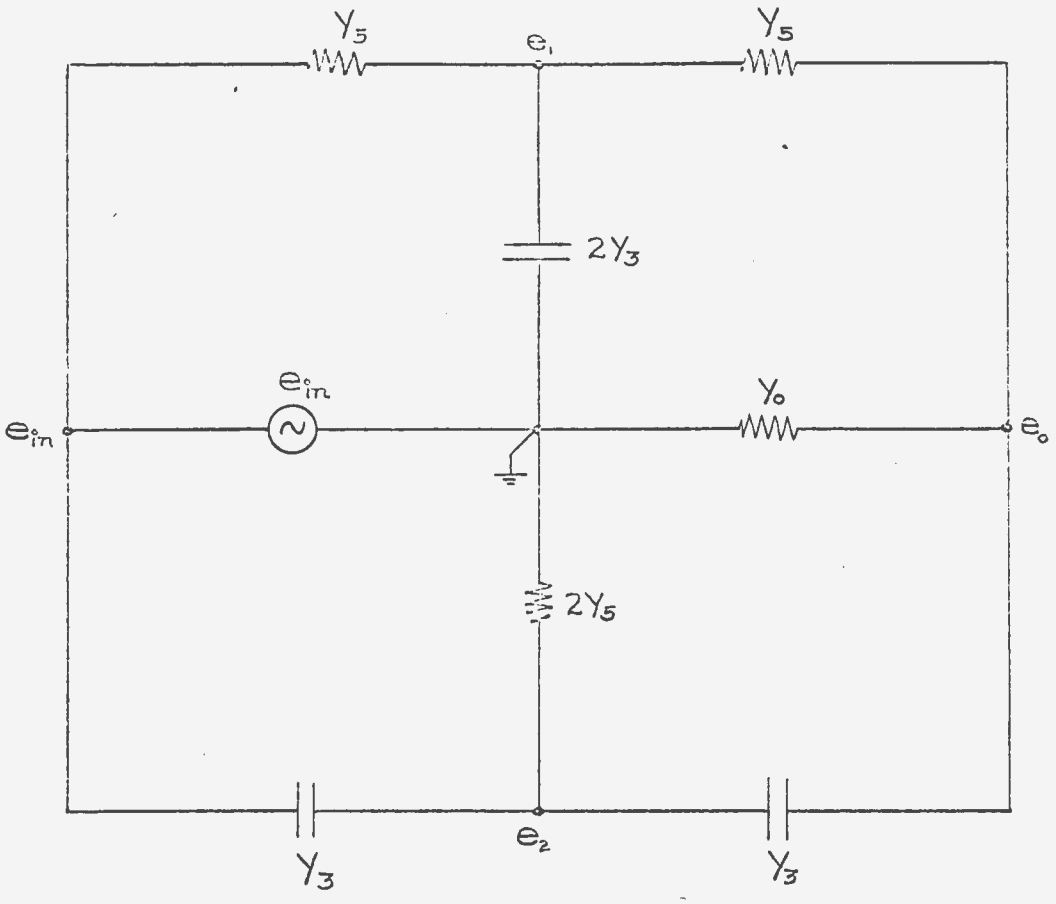

Figure 18. Parallel-tee filter circuit

The expression for the voltage transfer is:

$$\frac{e_o}{e_{in}} = \frac{\begin{vmatrix} -[2Y_5 + 2Y_3] & [0] & -[Y_5] \\ [Y_5] & [Y_3] & [0] \\ [0] & -[2Y_3 + 2Y_5] & -[Y_3] \end{vmatrix}}{\Delta}$$

$$\frac{e_o}{e_{in}} = \frac{Y_3^2[2Y_5 + 2Y_3] + Y_5^2[2Y_3 + 2Y_5]}{-Y_3^2[2Y_5 + 2Y_3] - Y_5^2[2Y_3 + 2Y_5] + [2Y_3 + 2Y_5]^2[Y_o + Y_3 + Y_5]}$$

$$\frac{e_o}{e_{in}} = \frac{Y_3^2 + Y_5^2}{Y_3^2 + Y_5^2 + 2Y_oY_3 + 2Y_oY_5 + 4Y_3Y_5}$$

Substituting $Y_o = 1/R_o$, $Y_3 = -j\omega C$, and $Y_5 = 1/R$ yields

$$\frac{e_o}{e_{in}} = \frac{R_o[1 - \omega^2 C^2 R^2]}{[R_o(1 - \omega^2 C^2 R^2) + 2R] - j[2\omega C R(R + 2R_o)]}$$

The voltage transfer and phase characteristics of any parallel tee filter circuit driven from a low source impedance can be computed from this equation for any loading of the filter.

APPENDIX B

Noise Measurements

The measurement of noise is a challenging problem in itself. Noise measurement requires an amplifier, a bandwidth determining device, and an AC voltmeter. The first two requirements can be satisfied by a narrow-band amplifier. The accuracy of noise measurements depends on the type of AC voltmeter used. Making the choice requires a knowledge of the reaction of the three common types of meters to noise voltages (5). The possible meter choices are: peak-responding, average-responding, and rms-responding.

The peak-responding meter responds to the highest peak of a noise waveform; however, the meter indication seldom reaches the actual peak due to damping within the meter. In general, the peak-responding meter reads noise 3 to 5 times higher than the actual rms value. Since the noise peaks vary in amplitude, the reading on a peak-responding meter will not be constant which makes it difficult to measure noise accurately.

The average-responding meter has the advantage that it reads the average value of the noise, which is generally constant. Probability analysis shows that the average value of noise is 0.8862 times the true rms value.

The rms-responding meter, of course, yields the most accurate noise measurement. This must be a true rms meter not a sine wave rms meter.

The noise data presented for the 2N2386, 6DS4, and 6AC7 was obtained using the system shown in Figures 19 and 20. The rectified and filtered

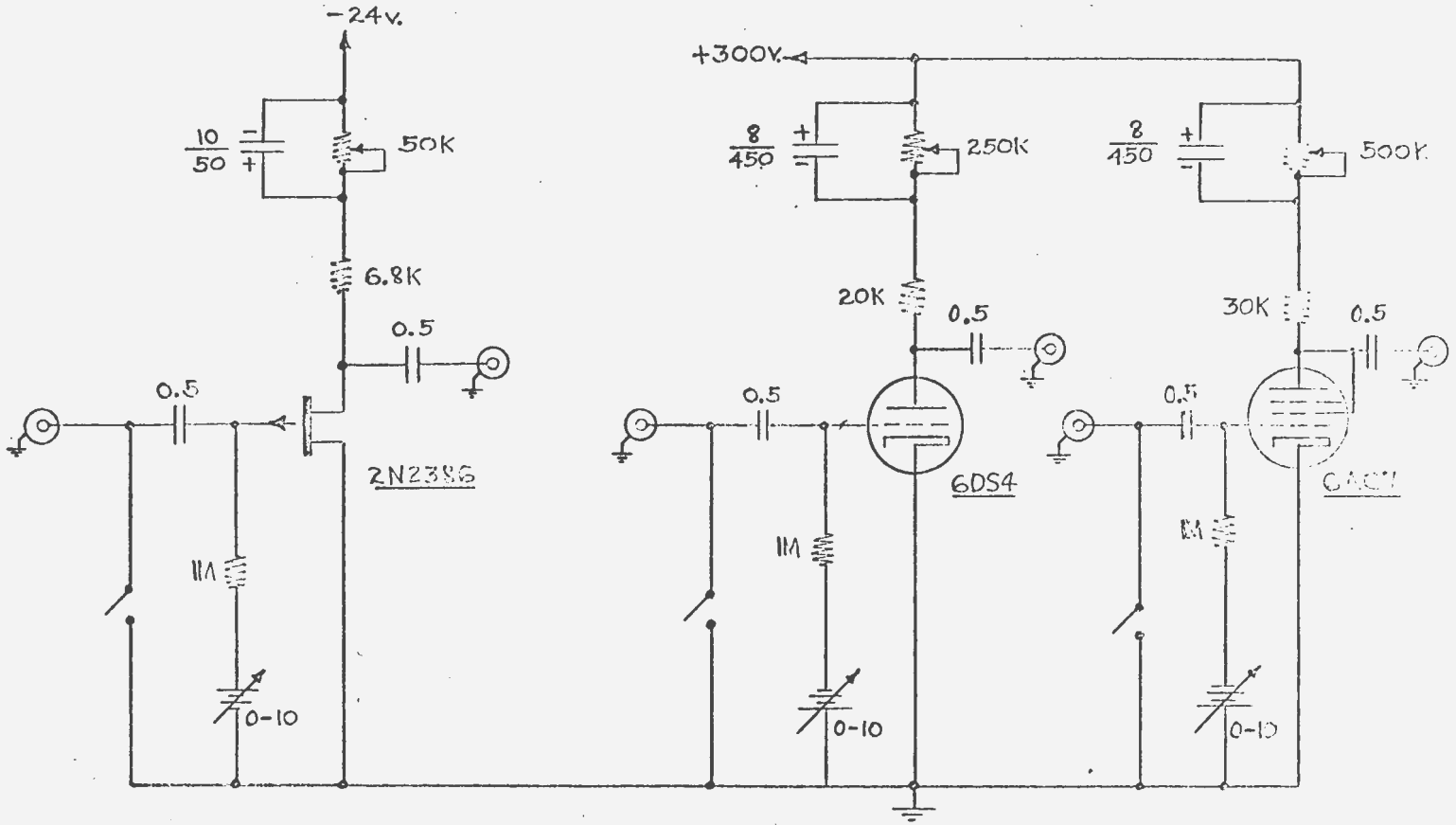

Figure 19. Component noise test circuit

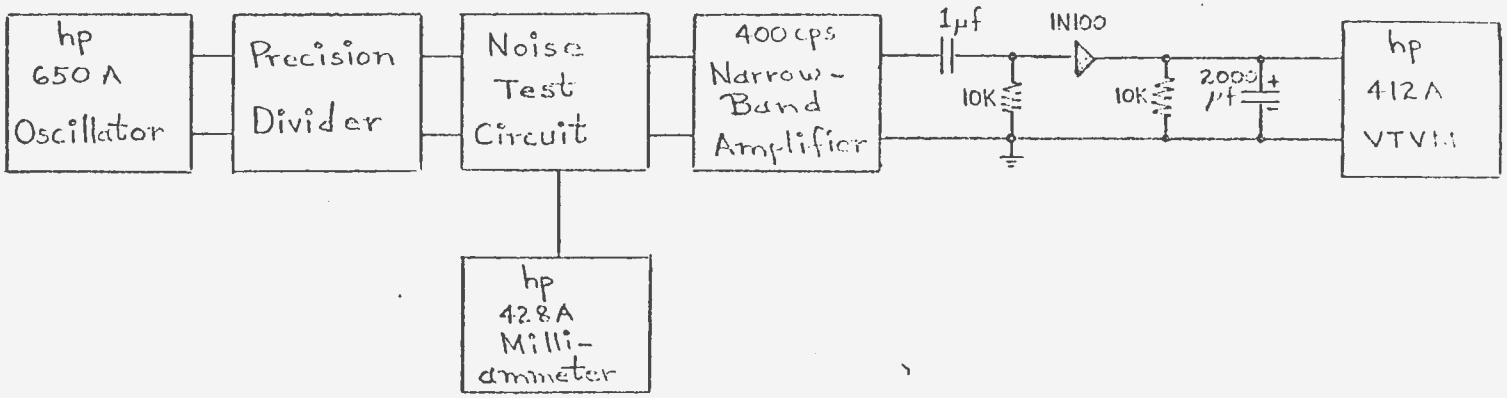

Figure 20. Overall noise measurement system

value of the noise was read on a DC meter in the absence of an rms-responding meter. The narrow-band amplifier used was the 400 cps unit described in reference 1. The component test circuits were designed to permit the variation of the DC conditions without varying the AC equivalent circuit.

The effective input noise of the amplifiers was measured with a true rms voltmeter. Since the rms value of the noise out of the amplifier was not constant, the figures recorded were the median rms value.